50 GHz High Output Voltage Distributed Amplifiers for 40 Gb/s EO Modulator Driver Application

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Abstract — **Both single-ended and differential distributed amplifiers were developed using 0.15 um GaAs power PHEMT for 40 Gb/s EO modulator driver circuits. The single-ended approach has achieved 12 dB gain up to 50 GHz, greater than 5 dB gain control range and output voltage > 6.5 Vp-p measured at 10 Gb/s. Power transfer data shows Psat of 20 dBm at 40 GHz, which translates to 6.3 Vp-p swing at 40 GHz. The differential approach has achieved 8 dB gain up to 45 GHz and differential output voltage of 9 Vp-p measured at 10 Gb/s. These amplifiers are suitable for use in fiber-optic communication systems.**

I. INTRODUCTION

As fiber communication systems move from OC-48 (2.5 Gb/s) to higher bit-rates of OC-192 (10 Gb/s) and future OC-768 (40 Gb/s) systems, high speed optical and electrical components that work above 40 GHz are essential. The external EO modulator is a key component in optical transmitters for long haul communication due to its superior performance (low loss, low chirp, high power handling and high extinction ratio). 40 Gb/s EO modulators with either single-ended drive or differential drive have been developed by various companies in the past two years. They all demand high drive voltage such as > 6 Vp-p for single-ended type or > 4 Vp-p for each port of differential type at 40 Gb/s. In addition, the EO modulator driver module needs to have 20-30 dB gain up to 50 GHz with greater than 6 dB gain control range in order to amplify the multiplexer output to the drive level required by the EO modulator. The 40 Gb/s EO modulator driver circuit is among the most difficult to design due to the extremely wide bandwidth, high speed, high gain and high output voltage requirements.

Several single-ended amplifiers with high drive capability for 40 Gb/s EO modulators have been developed in recent years [1]-[4]. All used GaAs power PHEMT devices with distributed amplifier circuit approach. This is because of the high cutoff frequency, high gain and high power characteristics of sub-micron GaAs power PHEMT and the extreme broadband capability of distributed amplifier. Measured 8 Vp-p output at 40 Gb/s was reported in [4] by cascading two MMIC chips: one power divider amplifier and one power combiner amplifier.

Differential driver amplifiers for 40 Gb/s application were reported using either GaAs HEMT with 2.9 Vp-p output from each port measured at 40 Gb/s [5] or using InP DHBT with 4.5 Vp-p differential output [6] measured at 40 Gb/s.

This paper describes a singled-ended distributed amplifier with a small chip size of 1.6 mm x 0.75 mm (which translates to low chip cost), high bandwidth (> 50 GHz, which means it's suitable for RZ and FEC applications at 40 Gb/s), high gain (12 dB), low power consumption (0.75W), high gain efficiency (16 dB/W) and high output voltage swing (> 6.5 Vp-p measured at 10 Gb/s, and > 6 Vp-p measured at 40 GHz). Two differential distributed amplifiers were developed with an 8 dB small signal gain up to 45 GHz. The measured differential output voltages at 10 Gb/s for the pre-amplifier and driver amplifier are 7 Vp-p and 9 Vp-p with power consumptions of 0.8 W and 1.1 W, respectively. This is the highest differential output voltage ever reported at these frequencies.

II. CIRCUIT DESIGN

The device used in the distributed amplifiers is 0.15 μm GaAs power PHEMT with ft of 90 GHz and fmax of 120 GHz. This device has a peak gm (at Vgs=-0.5V) of 510 mS/mm, Idss of 550 mA/mm, Idmax of 690 mA/mm (at Vgs=+0.5V), pinch-off voltage of -1.1 V and gate-drain breakdown voltage (at Igd=1mA/mm) around 10 V.

A. Single-Ended Distributed Amplifier:

The single-ended circuit design is a 4-cell distributed amplifier utilizing four 0.15 μm GaAs PHEMT unit cells. Each unit cell consists of two transistors with 100 μm gate width in a cascode configuration, as shown in Fig. 1a. A resistor was added in parallel to each drain line segment in order to improve stability. The gate and drain lines are terminated with a resistor in series with a small on-chip capacitor. In order to achieve flat gain down to

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low frequencies, a pad connected to the top plate of each on-chip termination capacitor is provided in order to attach a larger off-chip capacitor.

The gate bias should be applied either through an input bias-T or through the gate termination resistor. However, because of the higher current level, the drain bias should be applied either though an output bias-T or through an external inductor connected to a pad attached to the drain line. A third pad with a 500 ohm current limiting resistor is provided for the control voltage (second gate of the cascode) for gain control. A gain of 12 dB, input and output return losses better than 10 dB and group delay less than 15 ps from DC to 50 GHz were simulated.

The advantages of using cascode cells in the distributed amplifier are: 1) higher output shunt resistance reduces loading of the drain line (higher gain), 2) lower gate-to-drain capacitance reduces negative feedback at the high end (higher bandwidth), and 3) gain control is achieved.

B. Differential Distributed Amplifier:

The differential distributed amplifier consists of four differential unit cells connected by two gate lines and two drain lines. The differential unit cell consists of a pair of PHEMTs each with 80 µm gate width and with their common source connected to the drain of a PHEMT which acts as a current source. The gate of the current source PHEMT is grounded through a resistor and its source is connected through a source resistor to ground, as shown in Fig. 1b. The DC current of the unit cell is determined by the size of the current source PHEMT and its source resistor. The DC current can be adjusted by varying the source resistor of the current source PHEMT. The two gate lines and two drain lines are terminated with resistors in series with on-chip capacitors. Simulations showed 10 dB differential gain, better than 10 dB return losses, and less than 15 ps group delay from DC to 45 GHz.

III. Measured Circuit Performance

A. Single-Ended Distributed Amplifier:

Fig. 2 shows a photograph of the single-ended distributed amplifier with a chip size of 1.60 mm x 0.75 mm. The measured small signal gain (12 dB) and input return loss (> 8 dB) of four amplifiers biased at +6 V and 120 mA from 45 MHz to 50 GHz are shown on top of each other in Fig. 3. Fig. 4 shows power transfer curves measured at 25, 30, 35, and 40 GHz corrected for test fixture losses. When biased at 9V and 105 mA, this amplifier has a measured Psat of 20 dBm at 40 GHz, which translates to 6.3 Vp-p at 40 GHz. The measured eye diagram at 10 Gb/s indicates greater than 6.5 Vp-p output voltage swing with a power consumption of 0.75 W, as shown in Fig. 5. Due to test fixture problems and a non-optimized test setup, the measured 40 Gb/s eye diagram was not very good. Fig. 6 shows a good simulated 40 Gb/s eye diagram based on small signal measurements. Simulations, small signal measurements, and power sweep measurements all indicate that the 40 Gb/s eye diagram should be good when tested in an improved test setup.

B. Differential Distributed Amplifier:

A photograph of the differential distributed amplifier with a chip size of 2.2 mm x 0.85 mm is shown in Fig. 7. It has a measured differential gain of 8 dB and input and output return losses better than 8 dB from DC up to 45 GHz, as shown in Fig. 8. The measured output voltages at 10 Gb/s from two output ports for the pre-amplifier biased at 5 V, 160 mA is shown in Fig. 9. The differential output voltage swing for the pre-amplifier is greater than 7 Vp-p and the output voltage balance between the two output ports is better than 50 mV. The measured output voltages at 10 Gb/s from two output ports for the driver amplifier biased at 5 V, 230 mA is shown in Fig. 10. The differential output voltage swing for the driver amplifier is greater than 9 Vp-p.

IV. Conclusion

Both single-ended and differential distributed amplifiers were developed using 0.15 µm GaAs power PHEMT for 40 Gb/s EO modulator driver circuits. The single-ended approach has achieved 12 dB of gain up to 50 GHz, with greater than 5 dB of gain control and an output voltage swing of greater than 6.5 Vp-p measured at 10 Gb/s. Power transfer data shows Psat of 20 dBm at 40 GHz, which translates to 6.3 Vp-p swing at 40 GHz. The differential approach has achieved 8 dB gain up to 45 GHz and differential output voltage of 9 Vp-p measured at 10 Gb/s.

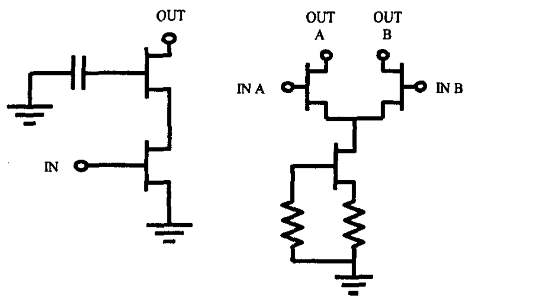

Fig. 1. (a) (Left) Schematic of cascode unit cell. and (b). (Right) Schematic of differential unit cell.

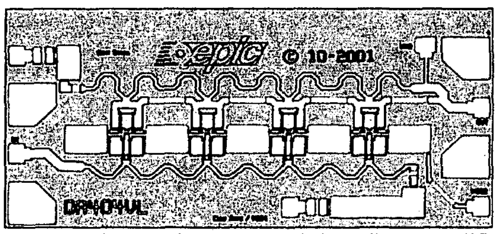

Fig. 2. Photograph of single-ended distributed amplifier.

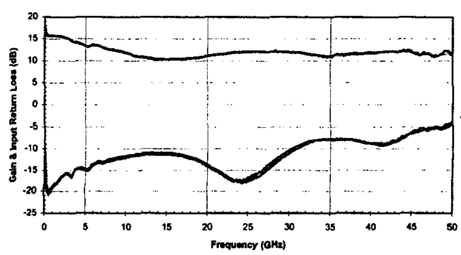

Fig. 3. Measured small signal gain and input return loss of four single-ended distributed amplifiers.

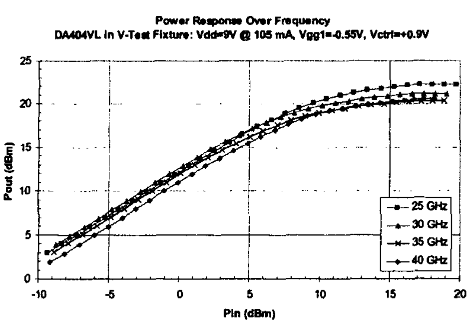

Fig. 4. Measured power transfer curves for the single-ended distributed amplifier from 25 to 40 GHz.

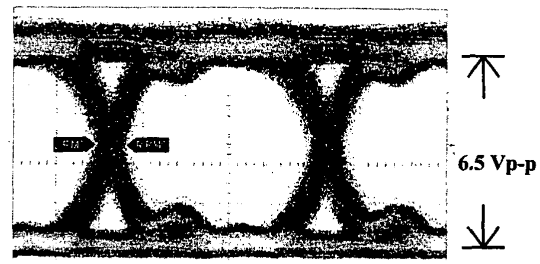

Fig. 5. Eye diagram of single-ended distributed amplifier measured at 10 Gb/s.

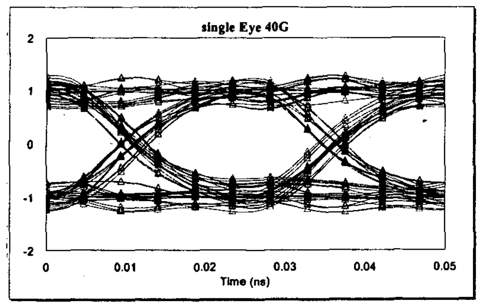

Fig. 6. Simulated small signal eye diagram of single-ended distributed amplifier at 40 Gb/s.

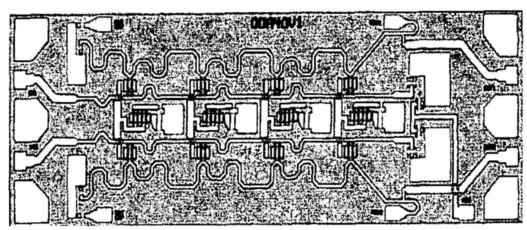

Fig. 7. Photograph of differential distributed amplifier.

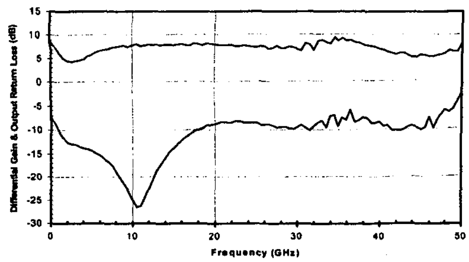

Fig. 8. Measured small signal differential gain and output return loss of differential distributed driver amplifier.

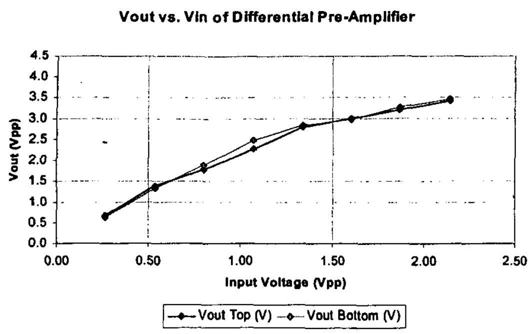

Fig. 9. Output voltage swings from two output ports of differential pre-amplifier measured at 10 Gb/s.

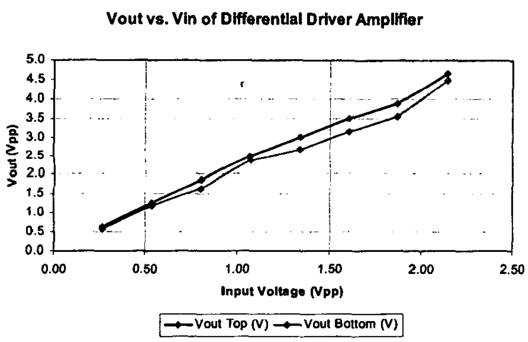

Fig. 10. Output voltage swings from two output ports of differential driver amplifier measured at 10 Gb/s.

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